R18

Code No: 155AA

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, January - 2025

ADVANCED COMPUTER ARCHITECTURE

(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) What is the significance of Amdahl's Law in context of parallel processing? [2]
b) Differentiate between centralized shared memory multiprocessors and distributed memory multiprocessors. [3]
c) List the different Scalability analysis approaches in parallel processing. [2]
d) What is Superscalar and Dynamic pipeline schedule? [3]
e) What are the problems faced in instruction pipeline? [2]
f) What do you mean by branch penalty? [3]
g) Differentiate the two different categories of protocols used for dealing with cache coherency problem. [2]
h) What are symmetric multi-core processor and asymmetric multi-core processor? [3]
i) What is Dataflow Architecture? [2]
j) What are the characteristics of Manchester Dataflow Machine? [3]

PART – B

(50 Marks)

2.a) In Uniprocessor computers systems, the Parallelisms can be achieved by balancing of subsystem bandwidth, multiprogramming and time sharing. Explain how does these mechanisms are implemented in such computers.
b) Explain the working principle of parallel processor architecture with distributed memory. List out its advantages and disadvantages. [5+5]

OR

3.a) Explain any two models of Parallel Processing with neat diagrams.
b) What is meant by Degree of parallelism? Explain Feng classification scheme to classify various computer architecture based on degree of parallelism. [5+5]

4.a) State Amdahl's law. Prove that frequent codes should make faster than the non-frequent one.
b) Assume that the memory access accounts for 70% of the execution time. What is the speedup by replacing a 150ns memory with a 30ns memory? How much fast is the new system? [5+5]

OR

5.a) What is the purpose of Delayed Load and Branch in RISC Pipeline? Use suitable example for your answer.

b) Explain the interleaved memory configurations in Parallel processors. [5+5]

6.a) List the class of applications for which Snooping cache coherence protocol would perform very poorly. Explain the state diagram of this protocol.

b) Consider the following reservation table for a pipeline having three stages S1, S2 and S3 and determine the Minimum Average Latency (MAL). [5+5]

Time -->

	1	2	3	4	5
S1	X				X
S2		X		X	
S3			X		

OR

7.a) Illustrate the possible configurations of PDP-10 multiprocessor.

b) Instruction execution in a processor is divided into 5 stages. Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write Back (WB). These stages take 5, 4, 20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementations of the processor are contemplated as:

i) A naive pipeline implementation (NP) with 5 stages and

ii) An efficient pipeline (EP) where the OF stage id divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.

Calculate the speedup (correct to two decimals places) achieved by EP over NP in executing 20 independent instructions with no hazards. [4+6]

8.a) Explain Shuffle Exchange and Omega networks with example.

b) Design a data routing network for an SIMD array processor with 256 PE's. Barrel cyclic shifters are used so that a route from one PE to another requires only one unit of time per integer-power-of –two shift in either direction.

i) Draw the interconnection barrel shifting network, showing all directly wired connections among the 256 PE's. In the drawing, at least one node (PE) must show all its interconnections to other PE's.

ii) Calculate the minimum number of routing steps from any PE_i to any other PE_{i+k} for the arbitrary distance $1 \leq k \leq 255$. Indicate also the upper bound on the minimum routing steps required. [4+6]

OR

9.a) Describe the components of a processing node in CM-5.

b) The twisted torus network of ILLIAC IV: Determine the diameter, average internode distance, and bisection width of the twisted torus network in the 8×8 ILLIAC IV configuration. What is the bisection bandwidth of this configuration? [4+6]

10.a) Illustrate processor-to-memory interconnection network of Cray Y-MP.

b) Explain the hybrid Architectures with illustrative example. [5+5]

OR

11.a) Explain distributed-memory machine with a butterfly multistage interconnection network emulating the PRAM.

b) Describe the different Latency-hiding techniques. [5+5]

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